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SE-7385

B. E. IV (ECC) (Sem. VII) Examination

May / June – 2011

Electronics System Design

Time : Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. - IV (ECC) (Sem. VII)**

Name of the Subject :

☛ **Electronics System Design**

☛Subject Code No. : **7 3 8 5** ☛Section No. (1, 2,.....) : **1, 2**

Seat No. :

Student's Signature

(2) Attempt al questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data whenever necessary and specify your assumptins clearly.
(5) use of scientific non-programmable calculator CASIO Fx 82, 83, 100 or equivalent of other makes is allowed.

SECTION - I

1 Do as directed. **20**

(i) Draw ideal transfer curve of voltage regulator. Justify the shape. **2**

(ii) Larger the value of K_p (Proportional mode controller constant), less value of error is required to saturate controller output. True of False ? Justify your answer. **2**

(iii) List units of integral mode controller constant and derivative mode controller constant, with its significance. **2**

(iv) Load current carrying capacity of fold back circuit is lower compared to simple short circuit protection for same series pass device. True or False ? Justify your answer. **2**

(v) The temperature has a range of 300K to 440K and a set point of 380K. Find the percentage of span error when measured temperature is 375K. **2**

(vi) Power consumption in linear voltage regulator is higher compared to switch mode power supply. True of false ? Justify your answer. **2**

(vii) Define following in context of process and control characteristics. **6**

(1) process equation (2) Dead time (3) process lag

(viii) Higher the value of filter capacitor, higher the value of ripple factor. True or false ? Justify your answer. **2**

2 (a) How fold back current limiting can be treated as improved version of constant current limiting ? **7**

(b) With the help of waveforms and diagram explain operation of buck type switching regulators; derive design equations and subsequently design regulator for output rating V_0=10V, I_0=4A and output ripple=200mV. Input voltage = 30 V and switching frequency for SMPS to be 45KHz. **8**

OR

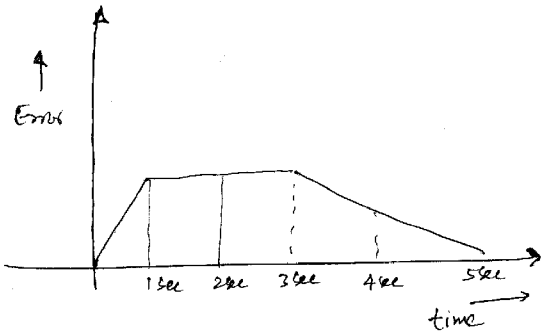
2 (a) It is expected to design voltage regulator circuit with a linear fold back characteristics that goes to a current limit of 20A at regulated output V_0=10V, and has short circuit limit of 7A. The unregulated input voltage has maximum value of 30V. **8**

(i) Draw output voltage versus output current.
(ii) Determine parameter of the linear fold back network.
(iii) Find the max power rating of the output transistor.
(iv) Find the output voltage and the output current at which the max power dissipation occurs.

(b) Describe operating principle of switch mode power supply, clearly justify how it regulates voltage against variation in supply voltage and load current. Draw buck and boost configuration of SMPs. **7**

3 (a) What do you mean by speed in float type controller? Differentiate single speed and multi speed float controllers. **5**

(b) Derive controller output for following error profile, if controller is of PD type and having parameters K_d=0.4s(D Mode), K_p = 5 (P Mode) and P_o = 15 %. Draw graph of controller output based on values of controller output. Desing and draw circuit of the controller. **5**



(c) It is required to design two possition controller with following data : **5**

For upper value of temperature: Switch off relay at 75 degrees and switch on 70 degrees for lower value of voltage : Switch off relay at 35 degrees and switch on degrees. Assume suitable scale factors for sensing speed. Explain each design steps and derive expressions you use.

SECTION - II

4 (a) Answer the followings : **12**

(i) State functions of EA' and PSEN' pins of 8051.

(ii) Explain the immediate addressing mode w.r.t.MOV instruction ?

(iii) State timer roll over value for mode 1 and 2.

(iv) What do you mean by simplex, full duplex and half duplex communication ?

(v) State vector locations for external hardware interrupts of 8051.

(vi) To interface external memory with 8051 which ports provide address and data line ? How ?

(b) Explain following 8051 instructions with suitable example. **04**

(i) DIV AB (ii) RR A

(c) Explain indirect memory addressing modes in 8051 w.r.t. MOV instructions. **04**

5 (a) Write a program to get hex data in the range of 00-FFH from PORT1 and convert it to decimal as unpacked BCD. Save the BCD digits in R7, R6 and R5 registers. **05**

(b) Write a program to generate square wave with 75% duty cycle on pin P0.5. What precaution is required while using 8051 ports as input ports ? **06**

(c) State steps of programming using polling method to program timers of 8051 in mode 2. **04**

OR

5 (a) Assume internal RAM memory locations 40-44H contains data. Search to see if any of the values equals 65H. If value 65H does exist, give the location of first searched byte to R4; otherwise make R4-00H. **05**

(b) What is difference between the RET and RETI instruction ? Explain why we can not use RET instead of RETI as the last instruction of an ISR ? **06**

(c) With the help of diagram explain how to program external hardware interrupts of 8051 ? **04**

6 Attempt any three. **15**

(a) Write a program to generate a 5ms pulse using timer 1. Take 12 MHz crystal frequency and neglect instruction overhead. Output square wave on pin p3.2.

(b) With the help of block diagram show how to connect PC serial with 8051. Also indicate baud rates supported by IBM PC.

(c) Explain function of SBUF and SCON registers for serial port programming.

(d) Give the interfacing of ADC 0809 with microcontroller 8051. Also write a program to read analog input and display the result in A.

(e) Explain interfacing of matrix keyboard with 8051 micro controller.
